Electronic Version
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Claims

[c1] 1. A chip package structure, comprising:
a carrier;
a chip, having an active surface with a plurality of bumps thereon, wherein the chip is bonded and electrically connected to the carrier in a flip-chip bonding process;
a heat sink, set over the chip, wherein the heat sink has a surface area greater than the chip; and
an encapsulating material layer, filling the bonding gap between the chip and the carrier and covering the heat sink and the carrier, wherein the encapsulating material layer is formed in a simultaneous molding process.

[c2] 2. The chip package structure of claim 1, wherein the package further comprises a plurality of standoff components set over the heat sink such that the height of the standoff components above the heat sink is equal to the thickness of the encapsulating material layer over the heat sink.

[c3] 3. The chip package structure of claim 1, wherein the package further comprises a thermal conductive adhesive layer set between the chip and the heat sink.

[c4] 4. The chip package structure of claim 1, wherein the encapsulating material layer has a thermal conductivity greater than 1.2 W/m.K.

[c5] 5. The chip package structure of claim 1, wherein the encapsulating material comprises resin.

[c6] 6. The chip package structure of claim 1, wherein the heat sink is fabricated using a metallic material.

[c7] 7. The chip package structure of claim 1, wherein the package further comprises an array of solder balls attached to a carrier surface away from the chip.

[c8] 8. The chip package structure of claim 1, wherein the package further comprises a passive component set on and electrically connected to the carrier.

[c9] 9. The chip package structure of claim 1, wherein the carrier is selected from a group consisting of a packaging substrate or a lead frame.

[c10] 10. A chip package structure, comprising:
a carrier;
a chipset, set over and electrically connected to the carrier, wherein the chipset comprises a plurality of chips, at least one of the chips is bonded to the carrier or another chip in a flip-chip bonding process so that a flip-

chip bonding gap is created;

a heat sink, set over the chipset, wherein the heat sink has a surface area greater than the chipset; and

an encapsulating material layer, filling the flip-chip bonding gap and covering the heat sink and the carrier, wherein the encapsulating material layer is formed in a simultaneous molding process.

[c11] 11. The chip package structure of claim 10, wherein the package further comprises a plurality of standoff components set over the heat sink such that the height of the standoff components above the heat sink is equal to the thickness of the encapsulating material layer over the heat sink.

[c12] 12. The chip package structure of claim 10, wherein the package further comprises a thermal conductive adhesive layer set between the top surface of the chipset and the heat sink.

[c13] 13. The chip package structure of claim 10, wherein the encapsulating material layer has a thermal conductivity greater than 1.2 W/m.K.

[c14] 14. The chip package structure of claim 10, wherein the chipset at least comprises:

a first chip, having a first active surface, wherein the first

chip is attached to the carrier such that the first active surface is positioned away from the carrier; and

a second chip, having a second active surface with a plurality of bumps thereon, wherein the second active surface of the second chip is bonded and electrically connected to the first chip in a flip-chip bonding process such that the bumps between the second chip and the first chip set up a flip-chip bonding gap.

[c15] 15. The chip package structure of claim 14, wherein the chipset further comprises a plurality of conductive wires with ends connected electrically to the first chip and the carrier respectively.

[c16] 16. The chip package structure of claim 10, wherein the chipset at least comprises:

a first chip, having an active surface with a plurality of first bumps thereon, wherein the first active surface of the first chip is bonded and electrically connected to the carrier in a flip-chip bonding process such that the first bumps between the first chip and the carrier set up a flip-chip bonding gap;

a second chip, having a second active surface, wherein the second chip is attached to the first chip such that the second active surface is positioned away from the first chip; and

a third chip, having a third active surface with a plurality

of second bumps thereon, wherein the third active surface of the third chip is bonded and electrically connected to the second chip in a flip-chip bonding process such that the second bumps between the third chip and the second chip set up another flip-chip bonding gap.

[c17] 17. The chip package structure of claim 16, wherein the chipset further comprises a plurality of conductive wires with ends electrically connected to the second chip and the carrier respectively.

[c18] 18. The chip package structure of claim 10, wherein the encapsulating material comprises resin.

[c19] 19. The chip package structure of claim 10, wherein the heat sink is fabricated using a metallic material.

[c20] 20. The chip package structure of claim 10, wherein the package further comprises an array of solder balls attached to a carrier surface away from the chipset.

[c21] 21. The chip package structure of claim 10, wherein the package further comprises a passive component set on and electrically connected to the carrier.

[c22] 22. The chip package structure of claim 10, wherein the carrier is selected from a group consisting of a packaging substrate or a lead frame.